#6 Amdt A 1/8-12-98

PATENT APPLICATION
Q46364

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of
Yoshinori MATSUI
Application No: 08/916,280 Group Art Unit: 2511
Filed: August 21, 1997 Examiner: HOANG, H.
For: SEMICONDUCTOR MEMORY CIRCUIT

AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

In response to the Office Action (Paper No. 3) mailed February 4, 1998, please amend the above-identified application as follows:

IN THE CLAIMS:

2. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second group of memory cells, said memory cell blocks being arranged in a first direction;

a first amplifier block provided adjacently to one end of an arrangement of said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on said one end, and selectively transferring a data of one of said memory cells in said one of said first and second groups via a first internal data line extending in a second direction different from said first direction;

a second amplifier block provided adjacently to another end of said arrangement, coupled to one of said first and second groups in one of said memory cell blocks on said another end, and selectively transferring a data of one of said memory cells in said one of first and second groups via a second internal data line thereof extending in said second direction;

at least one third amplifier block arranged between said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks adjacent to one side thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to another side thereof, and selectively transferring a data of one of said groups coupled thereto via a third internal data line thereof extending along said second direction;